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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,882	09/21/2006	Maxim B. Belotserkovsky	PU040085	5470

24498 7590 02/10/2009

Robert D. Shedd
Thomson Licensing LLC
PO Box 5312
PRINCETON, NJ 08543-5312

EXAMINER	
GHOWRWAL, OMAR J	

ART UNIT	PAPER NUMBER
2416	

MAIL DATE	DELIVERY MODE
02/10/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,882	BELOTSERKOVSKY, MAXIM B.	
	Examiner	Art Unit	
	OMAR GHOWRWAL	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 15 is objected to because of the following informalities: in the second limitation "derorated" should be "derotated". Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim(s) 1-7 is/are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to particular machine, or (2) transform underlying subject matter (such as an article or material) to a different state or thing. See page 10 of In Re Bilski 88 USPQ2d 1385. The instant claims are neither positively tied to a particular machine that accomplishes the claimed method steps nor transform underlying subject matter, and therefore do not qualify as a statutory process. The claimed method including steps of actions within a receiver is broad enough that the claim could be completely performed mentally, verbally or without a machine nor is any transformation apparent. For example even though the preamble of the independent claims 1 and 5 discloses a method for use in a receiver, the specification at para. 0031, page 10, teaches that a receiver can be implemented in software per se. (i.e. not a device/apparatus).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1, 5, 8, 13** are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Publication No. 2002/0067778 A1 to *Ahn*.

As to **claim 1**, *Ahn* discloses a method for use in a receiver, the method comprising:

processing a received signal with a phase-locked loop (PLL) (fig. 5, para. 0042, para. 0067, processing received signal 11, and PLL 105);

and generating a carrier frequency offset estimate as a function of a phase error signal of the PLL (fig. 5, para. 0042, obtaining a phase error, and extracting a polarity of the phase error and extracting a corresponding frequency offset by making use of polarity of the phase error).

As to claim 5, *Ahn* further discloses the method of claim 1, further comprising the step of updating the PLL with the carrier frequency offset estimate (fig. 5, para. 0042, generating digital type sine and cosine waves according to the extracted frequency offset, these waves being part of the PLL, hence it is updated).

As to **claim 8**, *Ahn* discloses a receiver (fig. 5) comprising:

a carrier tracking loop (CTL) for processing a received signal (para. 0096, specifically, two PLLs are provided in the carrier restoration section 100. For example,

the carrier restoration section 100 is composed of the PLL section 104 for frequency acquisition for acquiring the frequency offset and the PLL section 105 for phase tracking for tracking the residual phase jitter);

and a processor for estimating a carrier frequency offset as a function of a phase error signal of the CTL (fig. 5, para. 0096-0097, at this time the phase/frequency detector 101 is commonly used by the PLL section 104 for frequency acquisition and the PLL section 105 for phase tracking. Also, the phase/frequency detector 101 extracts the polarity by obtaining the phase error, and then expresses the phase error by the polarity, para. 0042, extracting a corresponding frequency offset by making use of polarity of the phase error).

As to claim 13, *Anh* discloses an integrated circuit (fig. 5) comprising:

a carrier tracking loop (CTL) for processing a received signal (para. 0096, specifically, two PLLs are provided in the carrier restoration section 100. For example, the carrier restoration section 100 is composed of the PLL section 104 for frequency acquisition for acquiring the frequency offset and the PLL section 105 for phase tracking for tracking the residual phase jitter);

and at least one register for use in setting an operating mode of the CTL (fig. 5, para. 0069, lock detection section 14 determines an operation mode of phase/frequency detector), wherein at least one operating mode of the CTL estimates a carrier frequency offset from a phase error signal of the CTL (fig. 5, para. 0071, phase/frequency detector calculates phase error in two modes, para. 0043, phase/frequency detection mode obtains phase error in order to acquire the frequency offset).

5. **Claim 14** is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,151,368 to *Cochran*.

As to **claim 14,** *Cochran* discloses an integrated circuit (fig. 2) comprising:

an input lead for receiving a signal (fig. 2, item 42);

and a carrier tracking loop (CTL) (fig. 2, item 56) for use in generating an open loop estimate (abstract, fig. 2, item 86, open-loop phase signal i.e. calculated based on frequency offset and is open loop, also one may take item 72 as the open-loop estimate since it is the frequency offset that is used in the open loop it leads to) of a carrier frequency offset (fig. 2, item 70, claim 12, phase integrator generates frequency offset) of the signal from a phase error signal of the CTL (fig. 2, item 64, claim 12, frequency offset is from phase-constellation error signal, which is part of CTL 56).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 2-3, 10-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2002/0067778 A1 to *Ahn* in view of "A Digital Transmission System Using Quaternary Partial Response CPM Principle Structure and Measurement Results" to *Matzner et al.* ("*Matzner*").

As to claim 2, *Ahn* does not expressly disclose the method of claim 1, wherein the processing step includes the step of setting the PLL in an open loop mode of operation.

Matzner discloses on page 734, the behavior of the closed loop becomes unpredictable and a frequency offset will never be compensated, therefore a different approach is needed which uses an open-loop.

Ahn and *Matzner* are analogous art because they are from the same field of endeavor regarding phase locked loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the open-loop as taught by Matzner into the invention of Ahn. The suggestion/motivation would have been to compensate for unpredictable behavior (Matzner, page 734).

As to claim 3, *Ahn and Matzner* further disclose the method of claim 2, wherein the generating step includes the steps of:

determining a rollover count value for the phase error signal (Matzner, fig. 3, "wrap around" from max to min of phase error);

determining a symbol count value of the received signal (page 734, "six symbols", which is a value pertaining to received signal, also, frequency offset is based on degrees per symbol, i.e. one symbol is also a symbol count value);

and generating the carrier frequency offset estimate from the determined rollover count value and determined symbol count value (Matzner, page 734, fig. 3, "six symbols" and frequency offset changes from 2 degrees/symbol to 30 degrees/symbol,

also the gradient (difference between phase error estimates, i.e. "wrap around", and since these are based on degrees per one symbol, the symbol count is also used) of the saw-tooth curve in fig. 3 is proportional to frequency offset, and this is used to estimate phase difference per symbol, i.e. frequency offset). In addition, the same suggestion/motivation of claim 2 applies.

As to claim 10, *Ahn* discloses a receiver (fig. 5) comprising:

a carrier tracking loop (CTL) for processing a received signal (para. 0096, specifically, two PLLs are provided in the carrier restoration section 100. For example, the carrier restoration section 100 is composed of the PLL section 104 for frequency acquisition for acquiring the frequency offset and the PLL section 105 for phase tracking for tracking the residual phase jitter);

and a processor for

(b) estimating a carrier frequency offset of the received signal as a function of a phase error signal of the CTL (fig. 5, para. 0096-0097, at this time the phase/frequency detector 101 is commonly used by the PLL section 104 for frequency acquisition and the PLL section 105 for phase tracking. Also, the phase/frequency detector 101 extracts the polarity by obtaining the phase error, and then expresses the phase error by the polarity, para. 0042, extracting a corresponding frequency offset by making use of polarity of the phase error);

(c) updating the CTL with the estimated carrier frequency offset (fig. 5, frequency offset used in feedback);

and (d) setting the CTL in a closed loop mode of operation (fig. 5, closed loop due to feedback).

Ahn does not expressly disclose (a) setting the CTL in an open loop mode of operation, estimating a carrier frequency offset of the received signal as a function of a phase error signal of the CTL *in the open loop mode of operation*.

Matzner discloses on page 734, the behavior of the closed loop becomes unpredictable and a frequency offset will never be compensated, therefore a different approach is needed which uses an open-loop. Furthermore, fig. 3 shows frequency offset being detected as a function of phase error signal.

Ahn and *Matzner* are analogous art because they are from the same field of endeavor regarding phase locked loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the open-loop as taught by Matzner into the invention of Ahn. The suggestion/motivation would have been to compensate for unpredictable behavior (Matzner, page 734).

As to claim 11, *Ahn* and *Matzner* further disclose the receiver of claim 10, wherein the CTL includes a rollover counter (Matzner, fig. 3, "wrap around" from max to min of phase error is a counted value) and a symbol counter (Matzner, page 734, "six symbols", which is a counted value pertaining to received signal, also, frequency offset is based on degrees per symbol, i.e. one symbol is also a symbol counted value) accessible by the processor for use in estimating the carrier frequency offset (Matzner, page 734, fig. 3, "six symbols" and frequency offset changes from 2 degrees/symbol to

30 degrees/symbol, also the gradient (difference between phase error estimates, i.e. "wrap around", and since these are based on degrees per one symbol, the symbol count is also used) of the saw-tooth curve in fig. 3 is proportional to frequency offset, and this is used to estimate phase difference per symbol, i.e. frequency offset). In addition, the suggestion/motivation of claim 10 applies.

8. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2002/0067778 A1 to *Ahn* and "A Digital Transmission System Using Quaternary Partial Response CPM Principle Structure and Measurement Results" to *Matzner et al.* ("*Matzner*") and in further view of U.S. 4,297,650 to *Shinmyo*.

As to claim 4, *Ahn and Matzner* further disclose the method of claim 3, further comprising the step of comparing the frequency offset estimate to a closed loop value of the PLL (Ahn, fig. 5, item 104-3, PLL PB_Data and oscillator with offset frequency values are inputted into frequency acquisition element).

Ahn and Matzner do not expressly disclose further comprising the step of *detecting a false lock condition* as a function of comparing the frequency offset estimate to a closed loop value of the PLL.

Shinmyo discloses a false lock in a PLL is due to the frequency offset linked to the modulation rate (sampling frequency fs), col. 1, lines 35-39.

Ahn, Matzner, and Shinmyo are analogous art because they are from the same field of endeavor regarding phase locked loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the false lock detection as taught by Shinmyo into the invention

of Ahn and Matzner. The suggestion/motivation would have been to eliminate false locks (Shinmyo, col. 1, lines 5-10).

9. **Claims 6-7** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,947,497 B1 to *Ahn* (*"Ahn_2"*) and "A Digital Transmission System Using Quaternary Partial Response CPM Principle Structure and Measurement Results" to *Matzner et al.* ("*Matzner*").

As to claim 6, *Ahn_2* discloses a method for use in a receiver (fig. 2), the method comprising:

running a carrier recovery loop (fig. 2-3) in an open loop mode;

generating an estimate of a carrier frequency offset of a received signal from a phase error signal of the carrier recovery loop (col. 3, lines 45-57, detected phase error leads to frequency offset);

updating an integrator of the carrier recovery loop with the estimate of the carrier frequency offset (fig. 2-3, item 28, col. 3, lines 53-67, equalizer coefficients update unit integrates results from equalizer 20, the phase lock signal (frequency offset) and phase lock detector 24 and sine wave from re-rotator 26);

and running the carrier recovery loop in a closed loop mode (fig. 2-3, loop is closed due to feedback of signals).

Ahn_2 does not expressly disclose running a carrier recovery loop in an *open loop mode*.

Matzner discloses on page 734, the behavior of the closed loop becomes unpredictable and a frequency offset will never be compensated, therefore a different approach is needed which uses an open-loop.

Ahn_2 and *Matzner* are analogous art because they are from the same field of endeavor regarding phase locked loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the open-loop as taught by Matzner into the invention of Ahn_2. The suggestion/motivation would have been to compensate for unpredictable behavior (Matzner, page 734).

As to claim 7, *Ahn_2 and Matzner* further disclose the method of claim 6, wherein the generating step includes the steps of:

determining a rollover count value for the phase error signal (Matzner, fig. 3, "wrap around" from max to min of phase error);

determining a symbol count value of the received signal (Matzner, page 734, "six symbols", which is a value pertaining to received signal, also, frequency offset is based on degrees per symbol, i.e. one symbol is also a symbol count value);

and generating the carrier frequency offset estimate from the determined rollover count value and determined symbol count value (Matzner, page 734, fig. 3, "six symbols" and frequency offset changes from 2 degrees/symbol to 30 degrees/symbol, also the gradient (difference between phase error estimates, i.e. "wrap around", and since these are based on degrees per one symbol, the symbol count is also used) of the saw-tooth curve in fig. 3 is proportional to frequency offset, and this is used to estimate

phase difference per symbol, i.e. frequency offset). In addition, the same suggestion/motivation of claim 6 applies.

10. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2002/0067778 A1 to *Ahn* in view of U.S. 4,297,650 to *Shinmyo*.

As to claim 9, *Ahn* further discloses the receiver of claim 8, further comprising comparing the frequency offset estimate to a closed loop value of the PLL (Ahn, fig. 5, item 104-3, PLL PB_Data and oscillator with offset frequency values are inputted into frequency acquisition element).

Ahn does not expressly disclose further comprising the step of *detecting a false lock condition* as a function of comparing the frequency offset estimate to a closed loop value of the PLL.

Shinmyo discloses a false lock in a PLL is due to the frequency offset linked to the modulation rate (sampling frequency fs), col. 1, lines 35-39.

Ahn and Shinmyo are analogous art because they are from the same field of endeavor regarding phase locked loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the false lock detection as taught by Shinmyo into the invention of Ahn. The suggestion/motivation would have been to eliminate false locks (Shinmyo, col. 1, lines 5-10).

11. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2002/0067778 A1 to *Ahn* and "A Digital Transmission System Using Quaternary Partial Response CPM Principle Structure and Measurement Results" to

Matzner et al. ("*Matzner*") and in further view of U.S. Publication No. 2002/0122511A1 to *Kwentus et al. ("Kwentus")*.

As to claim 12, *Ahn and Matzner* do not expressly disclose the apparatus of claim 10, wherein the receiver is a set-top box.

Kwentus discloses a satellite receiver in a set-top box that contains tracking loops (fig. 1, para. 0017, 0028).

Ahn, Matzner and Kwentus are analogous art because they are from the same field of endeavor regarding tracking loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the set-top box receiver as taught by Kwentus into the invention of Ahn and Matzner. The suggestion/motivation would have been to recover modulated signals in a wireless communications system (Kwentus, para. 0003).

12. **Claims 15-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,471,508 to *Koslov* in view of "A Digital Transmission System Using Quaternary Partial Response CPM Principle Structure and Measurement Results" to *Matzner et al.* ("*Matzner*").

As to **claim 15**, *Koslov* discloses apparatus (fig. 5) comprising:

a complex multiplier for multiplying a receive signal having a carrier frequency with a recovered carrier for providing a derotated signal (fig. 5, item 210);

a phase error detector responsive to the derotated signal for providing a phase error signal representative of phase errors between the derorated signal and target symbols selected from a predefined symbol constellation (fig. 5, item 233, col. 16, lines

5-20, phase detector, specifically one half of complex multiplier 233 therein, will determine a scalar phase error (.phi..sub.e) between de-rotated symbols Z.sub.REC and sliced symbols Z.sub.Q in the same manner as set forth above, the sliced symbols being from a QAM symbol constellation (col. 14, lines 15-16));

a loop filter for filtering the phase error signal to provide a filtered signal (fig. 5, item 240);

an integrator for integrating the filtered signal to provide an integrated signal (fig. 5, item 250);

a sin/cos table responsive to the integrated signal for providing the recovered carrier (fig. 5, item 260);

and a processor for updating the integrator with an estimate as a function of the phase error signal (fig. 5, item 237, phase error in the loop continually goes into loop filter then into phase accumulator 250, i.e. providing an update).

Koslov does not expressly disclose updating the integrator with *a carrier frequency offset estimate*.

Matzner discloses fig. 3 shows frequency offset being detected as a function of phase error signal.

Koslov and *Matzner* are analogous art because they are from the same field of endeavor regarding locked loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the frequency offset as taught by Matzner into the invention of

Koslov. The suggestion/motivation would have been to compensate for unpredictable behavior (Matzner, page 734).

As to claim 16, *Koslov and Matzner* further disclose the apparatus of claim 15, further comprising:

a rollover counter for counting a number of rollovers of the phase error signal (Matzner, fig. 3, "wrap around" from max to min of phase error is a number of rollovers);

and a symbol counter for counting a number of symbols in the derotated signal (Matzner, page 734, "six symbols", which is a value pertaining to received signal, also, frequency offset is based on degrees per symbol, i.e. one symbol is also a number of symbols);

wherein the carrier frequency offset estimate is generated from the counted number of rollovers and the counted number of symbols (Matzner, page 734, fig. 3, "six symbols" and frequency offset changes from 2 degrees/symbol to 30 degrees/symbol, also the gradient (difference between phase error estimates, i.e. "wrap around", and since these are based on degrees per one symbol, the symbol count is also used) of the saw-tooth curve in fig. 3 is proportional to frequency offset, and this is used to estimate phase difference per symbol, i.e. frequency offset). In addition, the same suggestion/motivation of claim 15 applies.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to OMAR GHOWRWAL whose telephone number is

(571)270-5691. The examiner can normally be reached on Monday-Thursday, 8:00am-5:00pm est..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derrick Ferris can be reached on (571)272-3123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/O. G./
Examiner, Art Unit 2416

/Derrick W Ferris/
Supervisory Patent Examiner, Art Unit 2416